NeuroSky®

Body and Mind. Quantified.

BMD101 DATA SHEET

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BMD101 Features and Benefits

High Performance Bio-Signal System-on-Chip (SoC)

- Single Chip Solution for accurate Bio-Signal Detection and Processing
- Mixed Signal SoC with Integrated Analog Front End (AFE), DSP functions and UART
- Accurate ECG raw signal as well as real-time heart-rate output
- Supports signal acquisition using dry contact electrodes

Advanced Analog Signal Processing

- High Performance AFE for detection and processing of Bio-Signal ranging from µV to mV Level
- Advanced Low-Noise Amplifier (LNA) and Anti-alias Filtering
- High Resolution (16-bit) ADC with 512 Bytes/sec. Sample Rate
- Low Input-Referred Noise
- Automatic Sensor-Off Detection
- Fully integrated high pass filter with DC offset correction

Powerful Digital Signal Processing

- Accurate on-chip heartbeat detection (24-200bpm) and real time heart rate (±1bpm) computation
- Strong notch filter with at least -60dB rejection for both 50Hz and 60Hz power supply noise
- Built-in low pass filter with stable band pass (0.5Hz - 100Hz)

Easy-to-use Interface

- UART (57600 Baud Rate) with 64 Byte TX FIFO
- Outputs raw data, real time heart rate, and sensor on/off status flag
- Can be very easily interfaced with external MCU and/or BLE/Bluetooth modules using UART

Low Power Consumption

- Uses a single external 3.3V (±10%) Power Supply and has a built in On-Chip 1.2V Regulator
- Low Operating current typically 0.8mA DC
- Power-down mode controlled by CS input

ESD Protection

- Industry standard 2KV (HBM) ESD protection on all pins
- External Diodes may be used on SEP and SEN to provide increased ESD protection (8kV Air Discharge, 4KV HBM)

Internal Clock

- Built-In RC Oscillator (±1% accuracy over entire operating range)

Small Form Factor

- 3mm x 3mm SON8 package

Multi-Platform SDK support

- Application Development framework for Android, IOS and Windows Platforms
- Available library of algorithms

Functional Description

As seen in Figure 1, BMD101 consists of three main sections:

Analog section consists of

- POR (Power-On-Reset)
- LDO (Low Drop Out regulator)
- DCO (Digitally Controlled Oscillator)
- AFE (Analog Front End) which consists of
  - HPF (High Pass Filter)
  - LOD (Lead-Off Detection)
  - LNA (Low Noise Amplifier)
  - ADC (16 bit Delta Sigma Modulator)

Digital section includes interfaces for

- Chip Select, (CS), Input
- RESET Input
- UART Interface (RX- Input, TX - Output)
- Lead On/Off status (LOD)
- Digitized Analog output signal (AFEOUT)

Configuration Section

contains factory programmed design parameters used by Analog and digital sections.

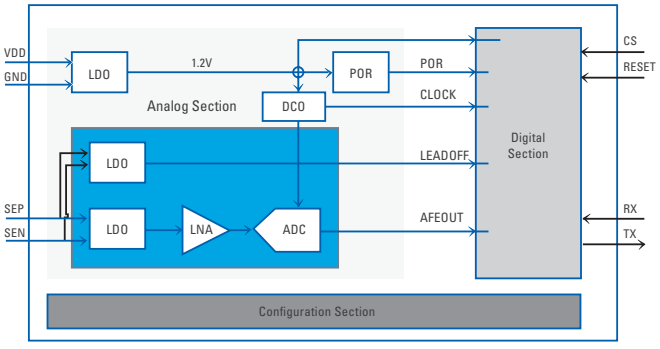


Figure 1 Block Diagram of BMD101

System Function

BMD101 is designed with an advanced analog front-end circuitry and it has a flexible, powerful digital signal processing structure. BMD101 can process bio-signal inputs ranging from μV to mV levels and is supported by NeuroSky proprietary SDK and algorithms to provide a complete solution.

The Low-Noise-Amplifier and ADC are the main components of BMD101 analog front end. Because of BMD101's extremely low system noise and programmable gain, it can detect and process bio-signals and convert them into digital words using a 16-bit high resolution ADC. The AFE also contains a sensor-off detection circuit.

The heart of BMD101 digital circuit is a powerful system management unit that is in charge of overall system configuration, operation management, internal/external communication, proprietary algorithm computation, and power management. BMD101 digital section also includes DSP blocks to accelerate calculations, such as various digital filtering, controlled by the configuration of the system management unit.

Target Applications

- BMD101 is designed for easy integration into Wearable Devices, Smart-Watches, Mobile Phones, Phone Accessories, Tablets etc. It can be embedded in to these devices or it can be used with Bluetooth/BLE to communicate wirelessly with these devices, as shown in Figure 2.

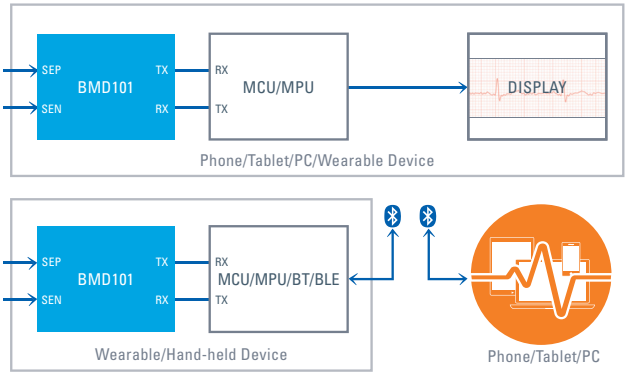


Figure 2 BMD101 Application Examples

Analog Front End

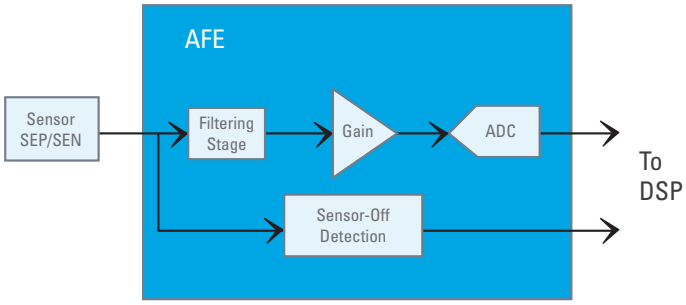


Figure 3: Block Diagram of AFE and its Interfaces to the Sensor and ASIC Digital Sections

The AFE receives low amplitude differential analog input signals. The DC offset and drift is removed by a fully integrated high pass filter (HPF). The signal is then amplified by a low noise amplifier (LNA) and its output is converted to a digital bit stream by the 16-bit ADC.

BMD101 has built-in sensor-off detection capability and any resistance between two sensor input pins that exceeds typically 25 Meg Ohms will trigger the sensor-off status.

Also, BMD101 contains an internal LDO voltage regulator which consists of a band-gap cell to generate a 1.2V reference followed by two separate unity gain buffers, for the analog and digital power supplies.

A digitally controlled oscillator (DCO) is included in BMD101 as well, which provides a fully integrated clock reference signal for internal use.

Digital Signal Processing (DSP) Circuits

The ADC output feeds into the DSP circuits as illustrated in Figure 3 and Figure 4.

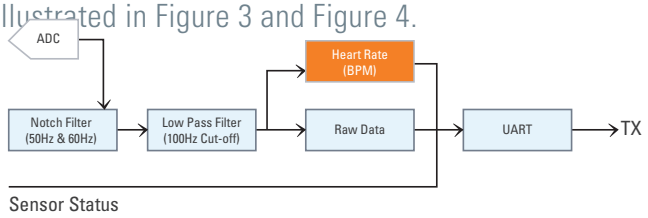


Figure 4: Digital Signal Processing Data Path

Part of bio-signal filtering in this system is done in the digital domain. It is expected that the main interference is due to the local power-supply noise and other noise artifacts.

Notch Filter

The Notch Filter is typically customized to reduce both 50Hz and 60Hz power noise so that it can be used anywhere in the world without reconfiguring. The notch rejection is typically -72.2 dB for both 60Hz and 50Hz.

Low Pass Filter

The Low Pass Filter has a 100Hz cutoff frequency. It provides a stable pass-band to the cutoff frequency, and -40dB at the high cutoff frequency.

Heart Rate Calculation

This block contains customized algorithms implemented in hardware for detecting each heart beat and computing real-time heart rate based on the time interval between successive beats.

Digital Output Data Format

The main digital communications interface of BMD101 is the UART, (TX/RX), interface. It's a standard UART interface that deploys a 1 start bit, 8 data bits, and 1 stop bit format.

The digital output packet of the UART/TX interface follows the pattern shown in Figure 5:

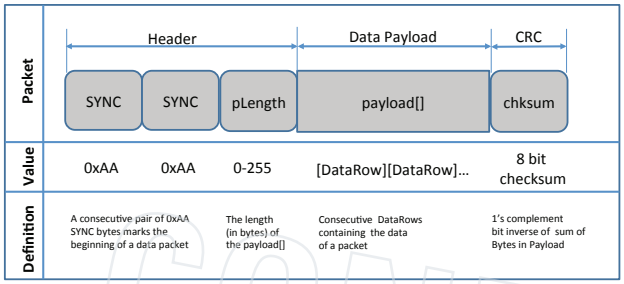


Figure 5: Output Data Packet Format

Packets are sent as an asynchronous serial stream of bytes. Each packet begins with its Header, followed by its Data Payload, and ends with its CRC checksum byte.

The Header of a Packet consists of 3 bytes: two synchronization SYNC bytes, (0xAA 0xAA), followed by a payload length pLength byte. The two SYNC bytes are used to signal the beginning of a new arriving Packet. The pLength byte indicates the length, in bytes, of the Packet's Data Payload.

The Data Payload of a Packet is simply a series of bytes. The number of Data Payload bytes in the Packet is given by the pLength byte from the Packet Header. The interpretation of the Data Payload bytes is defined in detail in the "Data Payload Format" section below. Note that the Data Payload should NOT be parsed until AFTER the CRC Checksum is verified.

The CRC Checksum of a Packet must be used to verify the integrity of the Packet's Data Payload.

The CRC Checksum is determined by:

1) Summing all the bytes of the Packet's Data Payload
2) Taking the lowest 8 bits of the sum
3) Performing the bit inverse (one's complement inverse) on those lowest 8 bits

A receiver that reads a Packet must recalculate the CRC Checksum of the Data Payload they received, and then compare it to the CRC Checksum byte that was received with the Packet. If the recalculated and received CRC values do not match, the entire Packet should be discarded as invalid. If they do match, then the Data Payload can be parsed.

Data Payload Format

The Data Payload consists of a continuous series of DataRows. Parsing a Data Payload involves parsing each DataRow until all the bytes of the Data Payload have been parsed.

A DataRow consists of bytes in the following format:

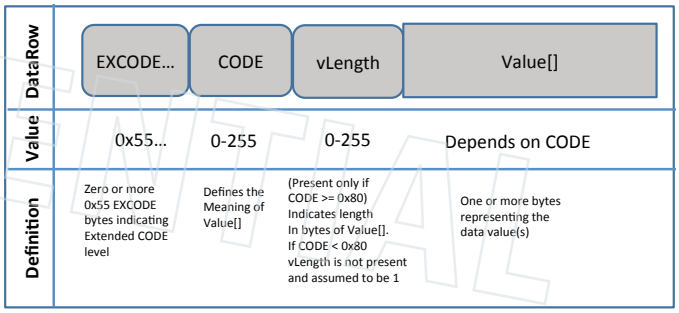


Figure 6 DataRow Format

The DataRow may begin with zero or more EXCODE (extended code) bytes, which are bytes with the value 0x55. The number of EXCODE bytes indicates the Extended Code Level. The Extended Code Level, in turn, is used in conjunction with the CODE byte to determine what type of data this DataRow contains.

The CODE byte indicates the type of data encoded in the DataRow. For example, a CODE of 0x03 indicates that the DataRow contains a heart rate value. For a list of defined CODE meanings, see the "CODE Definitions Table", (Table 1), on page 7. Note that the meaning of the CODE is dependent on the Extended Code Level and that neither the EXCODE byte of 0x55 nor the SYNC byte of 0xAA will ever be used as a CODE.

If the CODE byte is between 0x00 and 0x7F, then there will be no vLength byte. Also the Value[] byte immediately after the CODE is the 1-byte value and marks the end of the DataRow.

If, however, the CODE byte is between 0x80 and 0xFF, then it will be followed by a vLength byte indicating the number of bytes of DATA. These higher CODEs are used for:

a) Returning arrays of values,

b) Returning values that cannot fit in a single byte, or

c) Returning Values that need a varying number of bytes to be represented.

The format is defined in this way so that any properly implemented parser will not break in the future if:

1) If new CODEs representing arbitrarily long DATA values are added (they simply ignore unrecognized CODEs, but do not break in parsing),

2) If the order of CODEs is rearranged in the Packet, or

3) If some CODEs are not always transmitted in every Packet.

Extended Coded Level	CODE	[vLength]	Data Value Meaning
0	0x02	N/A	Signal Quality (0–sensor off, 200–sensor on)
0	0x03	N/A	Real-time Heart Rate (Beats Per Minute)
0	0x08	N/A	Don't Care
0	0x80	2	16-bit Raw Data (2's Complement)
0	0x84	5	Don't Care
0	0x85	3	Don't Care

Table 1 CODE Definitions Table

Reference Design Schematic

BMD101 has a single power input, VDD. To limit the noise that is injected into the ECG signal, power supply filtering/de-coupling is recommended.

- Pi Filter, as shown in Figure 7
- DC-DC Regulator output of 3.3V ±10%

Note: The power supply at VDD pin must be regulated with a smooth ramp from 0V to 2.5V that takes less than 10 µS.

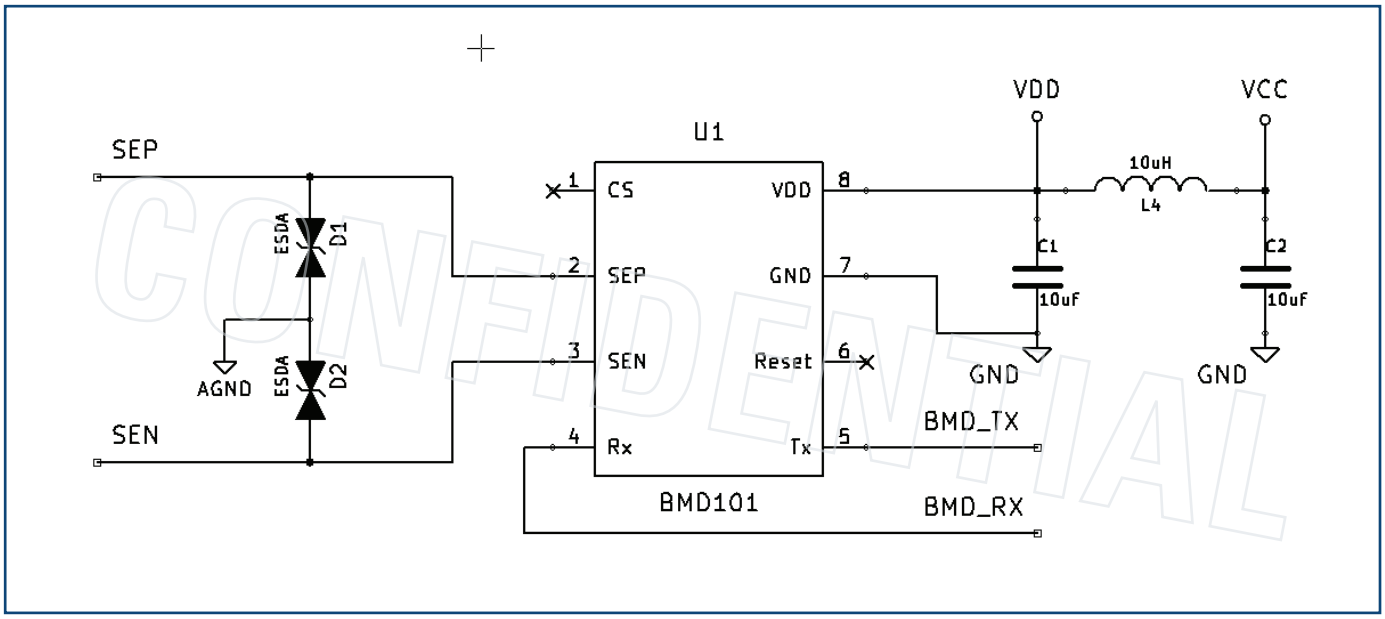


Figure 7 BMD101 Reference Design Schematic

CS and Reset pin can be pulled-up to VDD or connected to MCU GPIOs. RX and TX should be connected to either a microprocessor or a wireless communication chip for data transmission.

Reference Component	Recommend Value	Note
L4	10 µH	Pi Filter component
C1,C2	10 µF	Pi Filter components
D1,D2	For 4kV Contact Discharge and 8kV Air Discharge	ESD Diodes

Table 2 External Components on the Reference Design of Figure 7

Reference Design Schematic

Sensor Electrode Requirements

Sensor Material Options

- Silver-Silver Chloride (Ag-AgCl)
- Silver Coated Copper
- Gold
- Stainless Steel
- Conductive Fabric
- Conductive Rubber

Sensor Dimensions

- The recommended size of the Sensor is ~12mm diameter for circular shape or ~100 sq. mm area for rectangular shape

PCB Layout Guidelines

BMD101 is a mixed-signal device containing both analog and digital sections. Care must be exercised while doing PCB layout to make sure that proper grounding conventions are followed. Separate analog and digital ground planes should be used. These ground planes should join together only at the power supply ground. Digital signal traces should be shielded by digital ground. Sensor inputs must use shielded cable and be routed to the input pins using balanced traces in order to minimize impedance mismatch.

Electrical Characteristics

Absolute Maximum Ratings (1), (2), (3)

Symbol	Parameter	Min	Max	Units
VDD	Input Voltage	-0.1	3.6	V
V_{sense}	Analog Input Voltage , Differential Mode		1.0	Vp-p
T_{op}	Operating Temperature (4)	0	70	deg. C

Table 3 BMD101 Absolute Maximum Ratings

(1) The Absolute Maximum Ratings listed are the limits beyond which permanent damage to the device may occur. Continued normal operating performance is not guaranteed if the Absolute Maximum levels are exceeded.
(2) Unless otherwise noted, all Absolute Maximum Ratings listed apply within the normal BMD101 operating temperature range.
(3) The Absolute Maximum Ratings listed include only the BMD101. No external circuitry is included.
(4) Entire chip

BMD101 Specifications (1), (2), (3)

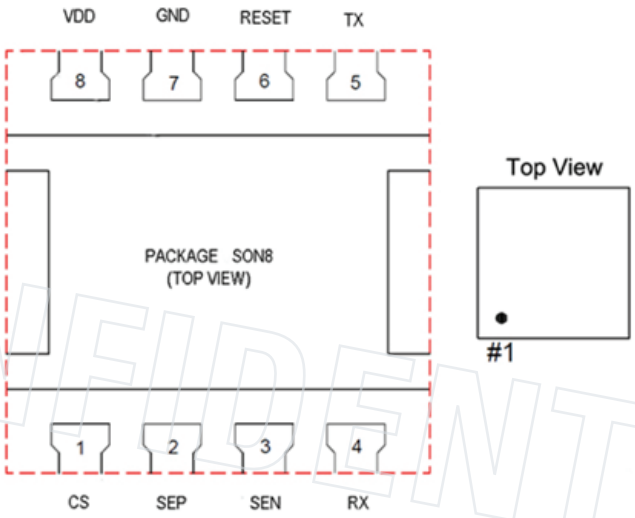
Symbol	Parameter	Min	Typical	Max	Units
VDD	Input Operating Power Voltage	2.5	3.3	3.6	V
t_{Ramp}	VDD Ramp Up Time			10	µsec
IDD	Input Operating Power Current	700	870	1100	µA
V_{OH}	Digital “1” Output Voltage	2.4		3.6	V
V_{OL}	Digital “0” Output Voltage	0		0.4	V
V_{IH}	Digital "1" Input Voltage	1.6		3.6	V
V_{IL}	Digital "0" Input Voltage	0		0.8	V
N/A	UART Baud Rate		57600		bits/sec.
V_{sense}	Differential Input Voltage			8	mVp-p
G_{Notch}	Notch Filter Gain (50 Hz and 60 Hz)	-62 (4)	-72.2	N/A	dB
F_{LCO}	Low Cutoff Frequency		0.5 (7)		Hz
F_{HCO}	High Cutoff Frequency		100		Hz
T_{op}	Operating Temperature (5)	0	25	70	deg. C
HBM	Analog Input ESD Voltage (6)			2000	V

Table 4 BMD101 Specifications

(1) Unless otherwise indicated, all parameter limits apply within the normal operating temperature range
(2) The limits listed include only BMD101. No external circuitry is included.
(3) Gain = 128 linear for all cases.
(4) With respect to Mid Band Gain, (Mid Band is 20 Hz)
(5) Entire ASIC
(6) (Human Body Model) per ANSI/ESDA/JEDEC JS-001-2010
(7) At room temperature

Packaging Information

Part No.	Order SKU	Status	Package I Pins	Qty	Eco Plan [1]	MSL, Peak Temp [2]	Storage Temp [3]
BMD101	80040-001	ACTIVE	SON I 8	490/Tray	Pb-Free (RoHS)	Level-3-260C-168 HR	5°C-30°C
BMD101	80040-301	ACTIVE	SON I 8	3000/Reel	Pb-Free (RoHS)	Level-3-260C-168 HR	5°C-30°C
BMD101	80040-051	ACTIVE	SON I 8	500/Reel	Pb-Free (RoHS)	Level-3-260C-168 HR	5°C-30°C



Terminal	Name	Function	Direction	Comment
1	CS	Power up or down control of LDO	Input	Active high
2	SEP	Positive ECG analog input	Input	
3	SEN	Negative ECG analog input	Input	
4	RX	UART RX	Input	
5	TX	UART TX	Output	
6	RESET	System reset pin	Input	Active low
7	GND	Ground	Supply	
8	VDD	3.3V power supply	Supply	

Figure 8 BMD101 Pin Diagram

Package Pin Assignments

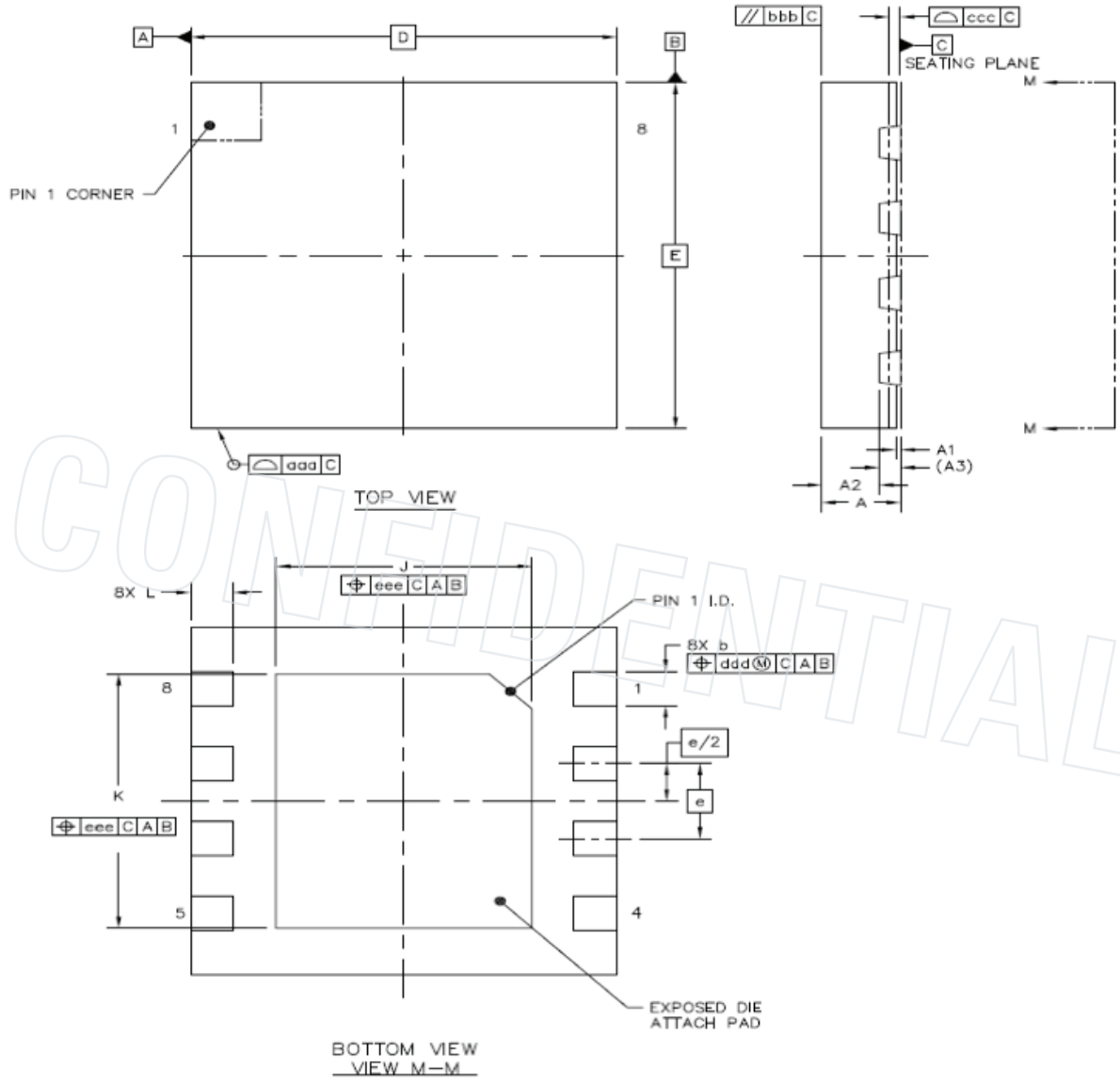
(1) Pb-Free (RoHS) – The term "Lead-Free" or "Pb-Free" means semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials.

(2) MSL, Peak Temp. – The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications and peak solder temperature.

(3) Recommended Temperature: room condition around 5 °C to 30 °C (can be stored for 1 year). Absolute short term storage temperature: -55 °C to 125 °C.

Appendix A

BMD101 SON8-3mm x 3mm x 0.6mm Package Outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.4	0.425
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.25	0.3	0.35
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.65 BSC	
EP SIZE	X	J	1.7	1.8	1.9
	Y	K	2.1	2.2	2.3
LEAD LENGTH		L	0.25	0.3	0.35
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	